General Digital Software Testing Process and Deliverables

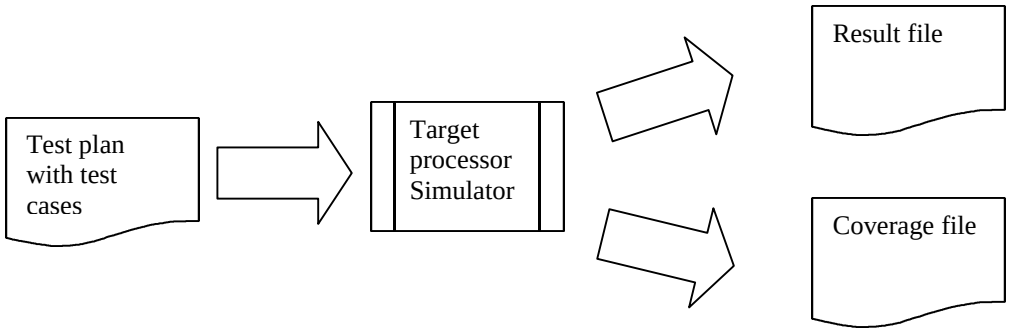
General Digital Software Quality Services offers software testing and quality assurance services to aid in the increasingly complex development of reliable software. The following example of our testing services and the associated deliverables are the type of service we offer to a client that develops real time embedded avionic software. For any given software, the requirements that must be met are subject to: a) the intended performance of the software indicated by a specification, and b) the safety or commercial impact of a software application failure.

This specific example of our testing services is done to meet the FAA's requirement for software unit testing called RTCA/DO-178B. This requirement demands that the unit test, which is a low level test, be performed on the software's assembly code.

A software test technician reviews the specification which may be in the form of a flow diagram or merely commented source code which must be "reverse engineered" by the technician to form an outline specification.

The technician then generates a test plan file consisting of test cases of various input/output scenarios needed to fulfill the (DO-178B) testing requirements for that unit. The test plan is then executed on a target processor simulator. The actual outputs are compared to expected outputs and code coverage is analyzed. Upon completion of the test, the test plan, result, and coverage files are electronically archived. Finally, the results of the test (pass/fail) and associated comments are tracked in a configuration manager.

The diagram below displays the process of test plan creation which is then run on a target processor simulator and the generation of a result file and a coverage file.



General Digital Software Quality Services is sensitive to the need to determine which requirements and techniques are best suited for the particular software developed. Our group can test software to accommodate a variety of requirements on different levels, from unit testing to integration testing, with a range of requirements from statement coverage to custom designed conditions. We work closely with your engineers, while maintaining bias-free organizational independence, to ensure full testing coverage for your release configuration. This includes the resolution of discrepancies found during the testing process as well as thorough documentation of test plans and results.

The result is a low impact off-loading of an entire verification phase yielding a net resource gain for your development team.

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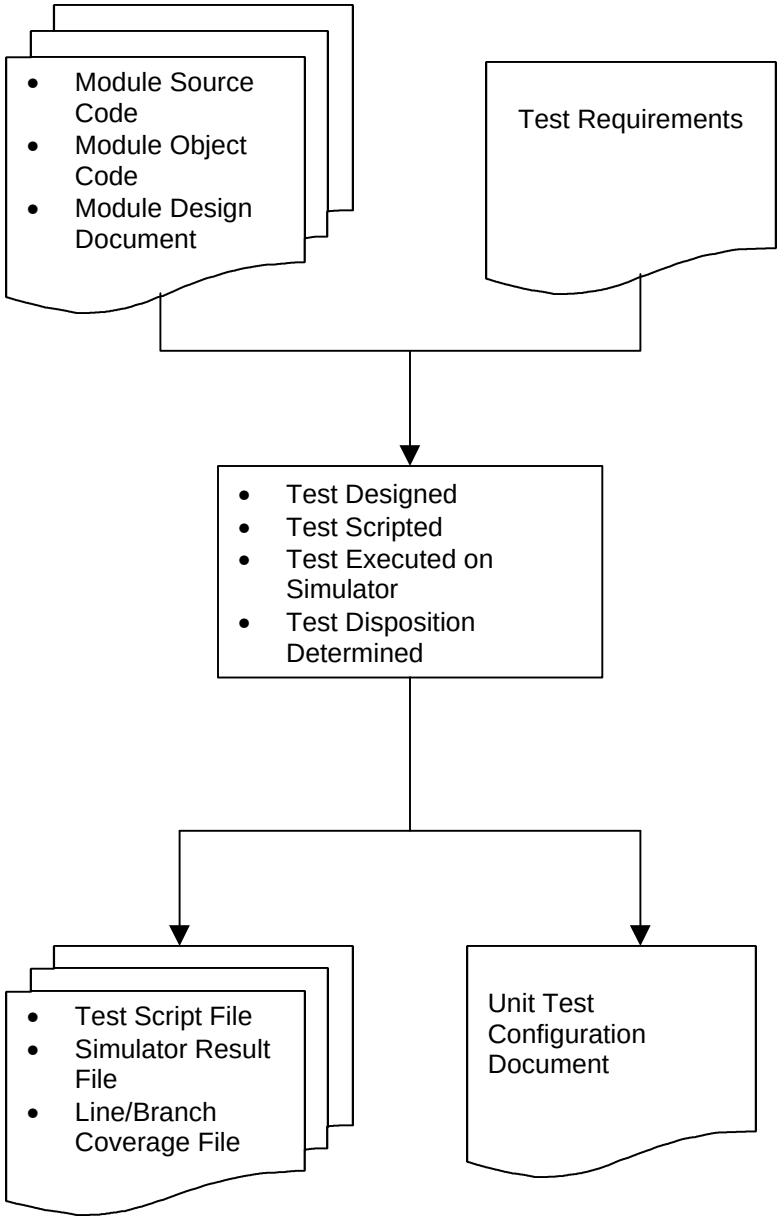
General Digital Unit Test Job Flow



General Digital Software Testing Process and Deliverables

The figures on the following pages display portions of the deliverable documents we provide to our existing clients in the form of electronic files and documents.

The figure below displays a test case within a test plan in electronic file form. The tester provides this file upon completion of a unit test.

```
*================================================  1.2  CALLER ===
*
* Setting Inputs...
SM CHANID 000001
SCL N1TIN 5.0 32768.0
SCL N1TINX 7.0 32768.0
SM N1TIND 000020
*
* Initialize Outputs...
SCL N1TPGIN 0.0 32768.0
SM N1TPGIND 000000
*
GO
*
* Verify Outputs...
* NAME=N1TPGIN SCALE=32768.0 VAL=5.0 TOL=3.000000000
CMP N1TPGIND 000020
*
*       VERIFY STORE TABLE BY DISPLAYING EXPECTED
*       VARIABLE ADDRESSES, IF ANY
```

The figure below displays a test case within a result file in electronic file form. Notice the trace of assembly code and the contents of various registers. The comparison of expected results versus actual occurs here also (i.e. 'VALUE IN RANGE:').

```
 ADDRESS|INSTR |OPERAND|OP ADDR|OP VAL|FLG|A REG|B REG |P SAV
 06 0075 SE             00 0000 000000 00 000000 000000 000000
 06 0077 LAA    1771    06 1771 100000 00 100000 000000 000000
 06 0100 AND    244     00 0244 076777 00 000000 000000 000000
 06 0101 SNE            00 0000 000000 00 000000 000000 000000
 06 0102 BRU    L0118   06 0107 043772 00 000000 000000 000000
 06 0107 LAA    1772    06 1772 177767 00 177767 000000 000000
 06 0110 AND    245     00 0245 000030 00 000020 000000 000000
 06 0111 STA    245     00 0245 000020 00 000020 000000 000000
 06 0112 BRU    @357    07 1601 041000 00 000020 000000 000000
 07 1601 NOP            00 0000 000000 00 000020 000000 000000
 -DM HALTER
 -* Verify Outputs...
 -* NAME=N1TPGIN SCALE=32768.0 VAL=7.0 TOL=3.000000000
 -* CSCL N1TPGIN 32768.0 4.000000000 10.000000000
 -CSCL 003155 32768.0 4.000000000 10.000000000
 VALUE IN RANGE:        7.00000
 -* CMP N1TPGIND 000020
 -CMP 000245 000020
 VALUE IN RANGE:                20
 -*
 -*     VERIFY STORE TABLE BY DISPLAYING EXPECTED
  -*     VARIABLE ADDRESSES, IF ANY
```

General Digital Software Testing Process and Deliverables

The figure below displays a coverage file in electronic form. Notice the analysis of instruction execution and branch execution. This file is also provided upon completion of a unit test.

```
                        LINE EXECUTION COVERAGE - Analyze Unit: ICS94
   Executed     Total   Percent  Analyze-unit
          3         3    100.00  ICS94\ICS94
                0 unit(s) excluded.
                INSTRUCTION EXECUTION COVERAGE - Analyze Unit: ICS94
Function: ICS94\ICS94.  Instruction(s) not executed:
    68    SHP := SCL_11_W'(SCL_26_L'(SCL_21_L'(Q * NP) * KSHPGR) / KSHP5252);
00032FEC 4E46              TRAP    #$6                 {BIVARIATE__1_P
0003300E 4E48              TRAP    #$8                 {BIVARIATE__1_P
00033010 600C              BRA.B   $3301E
0003305C 4E47              TRAP    #$7
0003305E 600A              BRA.B   $3306A
   Executed     Total   Percent  Analyze-unit
         57        62     91.94  ICS94\ICS94
                0 unit(s) excluded.
                BRANCH EXECUTION COVERAGE - Analyze Unit: ICS94
Function: ICS94\ICS94.  Branch(es) not executed:
    68    SHP := SCL_11_W'(SCL_26_L'(SCL_21_L'(Q * NP) * KSHPGR) / KSHP5252);
00032FEA 6802              BVC.B   $32FEE               Fall thru not taken.
0003300C 6804              BVC.B   $33012               Fall thru not taken.
0003305A 6804              BVC.B   $33060               Fall thru not taken.
Executed     Total   Percent  Analyze-unit
          7        10     70.00  ICS94\ICS94
                0 unit(s) excluded.
[End of file]
```

The figure below displays a document within the configuration manager which contains the test results (pass/fail) and any associated comments.

Program: MACH 3 JET Unit Test# 259

MODULE TEST COMPLETION REPORT

APPLICATION / SCN NUMBER : ENGINE CONTROLS/123
MODULE NAME : CONTROL_LOGIC
REVISION / VERSION : V1.0

TEST REMARKS (up to 100 lines) :

DISCREPANCY WITHIN THE FLOWCHART:

EROMNR: BIT 4 OF EROMIND WAS DECLARED AS AN INPUT BUT WAS NEVER USED IN THE FLOWCHART.

N1TPSEL: WAS DECLARED AS GLOBAL INPUT CHANGED BUT WAS NEVER CHANGED IN THE FLOWCHART.

Superseded by V2.0 UT379

Disposition : FAILED

Tested By: T. Rhodes Date: 7-JUL-1997